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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/795,939	03/08/2004	Sarath Kotamreddy	42P19124	1335

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BLAKELY SOKOLOFF TAYLOR & ZAFMAN
12400 WILSHIRE BOULEVARD
SEVENTH FLOOR
LOS ANGELES, CA 90025-1030

EXAMINER	
NGUYEN, HAU H	

ART UNIT	PAPER NUMBER
2628	

DATE MAILED: 04/18/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/795,939	KOTAMREDDY ET AL.	
	Examiner	Art Unit	
	Hau H. Nguyen	2628	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *03* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 January 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-32* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-32* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on January 27, 2006 has been entered.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1-5, 14-16, 19-21, 30-32 are rejected under 35 U.S.C. 102(e) as being anticipated by Gulick et al. (U.S. Patent No. 6,523,019).

Referring to claims 1, 2, 14, 19, 30, and 31, Gulick et al. teach a chipset 201 (col. 3, lines 34-43) as shown in Figs. 2 and 8, comprising a memory controller 202, a graphics accelerator 206 and a link interface 205 (a queue mechanism) which includes a first function unit block (FUB) (transmit controller 215) coupled to the graphics accelerator to perform a first set of functions for the queue mechanism and a second FUB (receiver controller 222) coupled to the memory controller to perform a second set of functions for the queue mechanism (col. 4, lines 30-34). As shown in Fig. 4, Gulick et al. teach each channel in the link layer includes FIFO and

queues (numerals 401-411) of addressing information and data that have been sent across the bus or that will be sent across the bus and that FIFOs and queues are designed to the specific requirements of the channels being serviced by the link (col. 4, lines 49-66). Thus, it is inherent that the first FUB and the second FUB are at a first and second physical partition on the chipset die, respectively. Gulick et al. teach the queue mechanism also includes a control logic (receive controller and transmit controller) to facilitate an interface between the graphics accelerator and the memory controller (col. 3, lines 21-23).

In regard to claims 3, 15, 20, and 32, Gulick et al. also teach the first FUB is operated based upon a first clock domain (Fig. 2, clk 211) and the second FUB is operated according a second clock domain (Fig. 2, clk 218) (col. 3, lines 10-20).

In regard to claim 4, Gulick et al. teach the signaling between the first FUB and the second FUB is unidirectional (col. 3, lines 21-23) and the link 209 transfers packet based information to and from a unit or function (col. 5, lines 34-45).

As for claims 5, 16, 21, as cited above, Gulick et al. teach the second FUB also comprising storage elements (FIFOs and queues) in which to store information that is written into the queue mechanism.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 6-13, 17-18, 22-29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gulick et al. (U.S. Patent No. 6,523,019) in view of Cavanna et al. (U.S. Patent No. 6,208,703).

Referring to claims 6-13, 17-18, 22-29, as cited above, Gulick et al. teach a queue mechanism comprising a first functional unit and a second functional unit, and further teach the link can provide control packets indicating a read or write operation (col. 6, lines 9-15) (load and unload pointers indicating a location to store/read information).

Thus, Gulick et al. all the limitations of claims 6-13, except for a logic to compare the load pointer and the unload pointer; the load pointer is clock crossed to the second clock domain; and the unload pointer is clock crossed to the first clock domain.

However, Cavanna et al. teach first-in-first-out synchronizer wherein, as shown in Fig. 1, comprises on the producer side (first FUB), the single stage FIFO synchronizer includes a write input 27, a write clock (WrtCLK) input 28 (first clock domain), a reset (NotWrtRST) input 29 and data (Din[3..0]) input 30. A NotFull output 26 indicates whether the single stage FIFO synchronizer is ready to receive more data from the producer (to determine a command is present). On the consumer side (second FUB), the single stage FIFO synchronizer includes a read input 19, a read clock (RdCLK) input 22 (a second clock domain), a reset (NotRdRST) input 23 and data (Din[3..0]) output 24. A not empty output 18 indicates whether the single stage FIFO synchronizer is ready to transfer more data to the consumer (to determine availability of storage elements). The single stage FIFO synchronizer includes a comparator 14 and 17 (a match logic for comparing read and write pointers), a synchronizer flip-flop 12, a synchronizer flip-flop 16 (clock gating means), a comparator 17, a write pointer flip-flop 11 (a load pointer), a read pointer flip-flop 21 (an unload pointer), connected as shown in Fig. 1 (col. 5, lines 36-55).

Cavanna et al. further teach the two signals (write pointer 32 and a read pointer 31) that cross the clock domain each have only one transition per handshake cycle (col. 6, lines 6-9). Data to be stored in the storage elements is directly flopped in the first clock domain within the second FUB in the consumer FIFO 122 via the synchronizer FIFO 103 as shown in Fig. 4, and col. 7,lines 25-35, and col. 8, lines 13-27.

Since Gulick et al. teach a control logic controlling a read pointer and a write pointer for accessing the memory, Cavann et al. teach synchronizing between read and write pointers operated in different clock domains as cited above, it would have been obvious to one skilled in the art to utilize the method as taught by Cavanna et al. in combination with the method as taught by Gulick et al. in order to permit faster operation of the interface (col. 4, lines 57-63).

Conclusion

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hau H. Nguyen whose telephone number is: 571-272-7787. The examiner can normally be reached on MON-FRI from 8:30-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kee Tung can be reached on (571) 272-7794.

The fax number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished

applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system contact the Electronic Business Center (EBC) at 866-2 17-9197 (toll-free).

H. Nguyen

4/14/2006

Kee M. Tung
Primary Examiner